FP2189

1 – Watt HFET

Product Information

Product Features

- 50 – 4000 MHz
- +30 dBm P1dB
- +43 dBm Output IP3
- High Drain Efficiency
- 18.5 dB Gain @ 900 MHz
- Lead-free/Green/RoHS-compliant SOT-89 Package
- MTTF >100 Years

Applications

- Mobile Infrastructure
- CATV / DBS
- W-LAN / ISM
- RFID
- Defense / Homeland Security
- Fixed Wireless

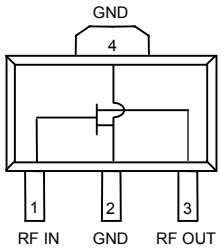
Product Description

The FP2189 is a high performance 1-Watt HFET (Heterostructure FET) in a low-cost SOT-89 surface-mount package. This device works optimally at a drain bias of +8 V and 250 mA to achieve +43 dBm output IP3 performance and an output power of +30 dBm at 1-dB compression, while providing 18.5 dB gain at 900 MHz.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The FP2189 has an associated MTTF of greater than 100 years at a mounting temperature of 85°C and is available in both the standard SOT-89 package and the environmentally-friendly lead-free/green/RoHS-compliant and green SOT-89 package. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high efficiency are required.

Functional Diagram



Function	Pin No.
Input / Gate	1
Output / Drain	3
Ground	2, 4

Specifications

DC Parameter	Units	Min	Typ	Max
Saturated Drain Current, I_{dss} (1)	mA	445	615	705
Transconductance, G_m	mS		280	
Pinch Off Voltage, V_p (2)	V		-2.1	

RF Parameter (3)	Units	Min	Typ	Max
Operational Bandwidth	MHz	50		4000
Test Frequency	MHz		800	
Small Signal Gain	dB		18.5	
SS Gain (50 Ω, unmatched)	dB	15		21
Maximum Stable Gain	dB		24	
Output P1dB	dBm		+30	
Output IP3 (4)	dBm		+43	
Noise Figure	dB		4.5	
Drain Bias			+8V @ 250 mA	

1. I_{dss} is measured with V_{gs} = 0 V, V_{ds} = 3 V.
2. Pinch-off voltage is measured when I_{ds} = 2.4 mA.
3. Test conditions unless otherwise noted: T = 25ºC, V_{DS} = 8 V, I_{DQ} = 250 mA in an application circuit with $Z_L = Z_{LOPT}$, $Z_S = Z_{SOPT}$ (optimized for output power).
4. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Performance (5)

Parameter	Units	Typical			
Frequency	MHz	915	1960	2140	2450
Gain	dB	18.7	15.6	14.4	13.0
Input Return Loss	dB	21	14.6	23	26
Output Return Loss	dB	8.3	12	11.5	9.6
Output P1dB	dBm	+30.2	+30.4	+30.6	+31.2
Output IP3 (4)	dBm	+42.8	+43.5	+43.9	+45.3
Noise Figure	dB	4.5	3.4	4.5	
IS-95 Channel Power @ -45 dBc ACPR	dBm	+24.5	+23.8		
W-CDMA Ch. Power @ -45 dBc ACLR				+22.2	
Drain Voltage	V	+8			
Drain Current	mA	250			

5. Typical parameters represent performance in a tuned application circuit.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
DC Power	4.0 W
RF Input Power (continuous)	6 dB above Input P1dB
Drain to Gate Voltage, V_{dg}	+14 V
Junction Temperature	+220° C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

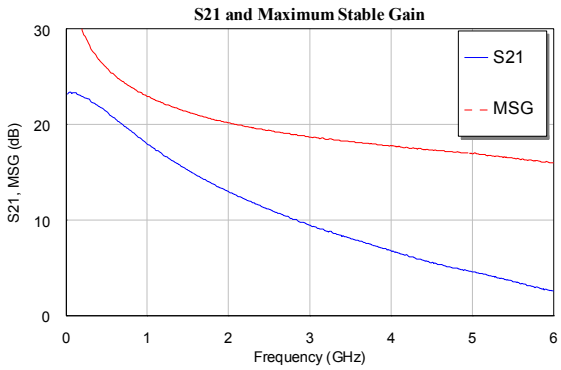
Part No.	Description
FP2189*	1 -Watt HFET (lead-tin SOT-89 Pkg)
FP2189-G	1 -Watt HFET (lead-free/green/RoHS-compliant SOT-89 Pkg)
FP2189-PCB900S	870 – 960 MHz Application Circuit
FP2189-PCB1900S	1930 – 1990 MHz Application Circuit
FP2189-PCB2140S	2110 – 2170 MHz Application Circuit

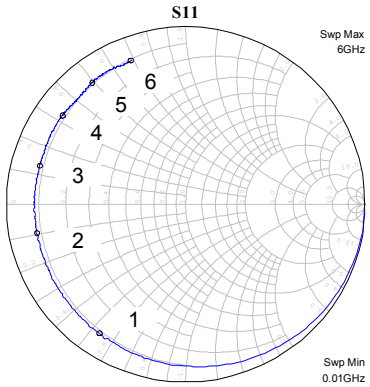
* This package is being phased out in favor of the green package type which is backwards compatible for existing designs. Refer to Product Change Notification WJPCN06MAY05TC1 on the WJ website.

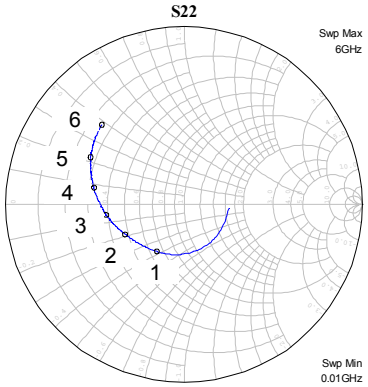
Specifications and information are subject to change without notice.

Typical Device Data

S-Parameters (V_{DS} = +8 V, I_{DS} = 250 mA, T = 25°C, calibrated to device leads)







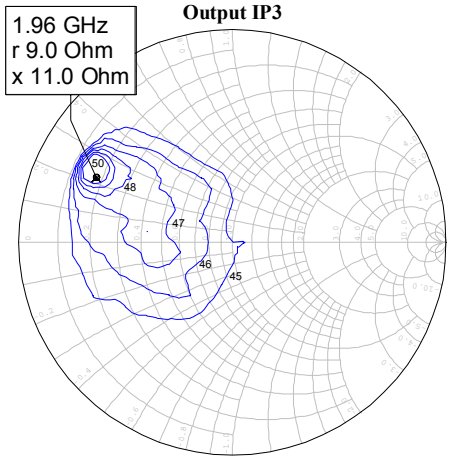
Note:
Measurements were made on the packaged device in a test fixture with 50 ohm input and output lines.
The S-parameters shown are the de-embedded data down to the device leads and represents typical performance of the device.

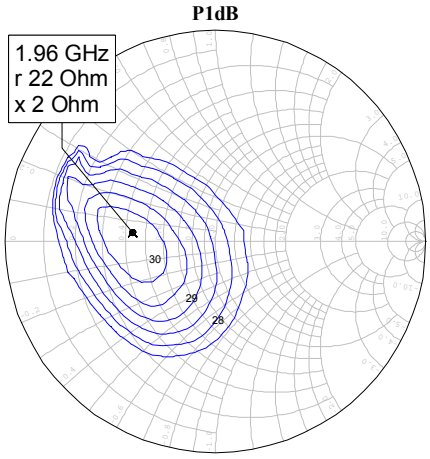
Freq (MHz)	S11 (mag)	S11 (ang)	S21 (mag)	S21 (ang)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)
50	0.995	-9.21	15.562	173.61	0.004	82.89	0.261	-10.68
250	0.963	-43.33	14.312	151.51	0.017	65.62	0.263	-46.04
500	0.906	-78.54	11.961	128.91	0.029	49.26	0.276	-81.01
750	0.876	-104.31	9.735	111.97	0.036	34.34	0.288	-103.33
1000	0.851	-123.00	8.046	98.87	0.040	24.98	0.300	-119.07
1250	0.836	-138.30	6.765	86.96	0.042	17.12	0.315	-130.86
1500	0.834	-149.84	5.864	77.58	0.043	12.50	0.330	-139.51
1750	0.825	-159.46	5.090	68.80	0.043	8.49	0.346	-147.68
2000	0.827	-168.49	4.556	60.62	0.044	4.05	0.368	-153.90
2250	0.827	-176.39	4.049	52.41	0.043	0.16	0.378	-160.68
2500	0.826	177.53	3.660	45.61	0.043	-1.33	0.394	-166.28
2750	0.830	171.26	3.336	38.11	0.043	-3.95	0.416	-171.43
3000	0.829	165.08	3.054	30.79	0.043	-6.46	0.427	-177.48
3250	0.828	159.79	2.779	24.59	0.043	-6.43	0.445	177.09
3500	0.836	154.28	2.596	18.29	0.043	-8.81	0.465	172.17
3750	0.838	149.19	2.422	11.82	0.044	-8.46	0.478	166.87
4000	0.839	144.09	2.276	5.12	0.044	-8.40	0.498	160.44

Device S-parameters are available for download off of the website at: http://www.wj.com

Load-Pull Data at 1.96 GHz

(V_{ds} = 8 V, I_{ds} = 250 mA, 25°C, Z_S = 50 Ω)





Maximum IP3 = +51 dBm at Z_L = 9 + j11 Ω

Maximum P1dB = +30.9 dBm at Z_L = 22 + j2 Ω

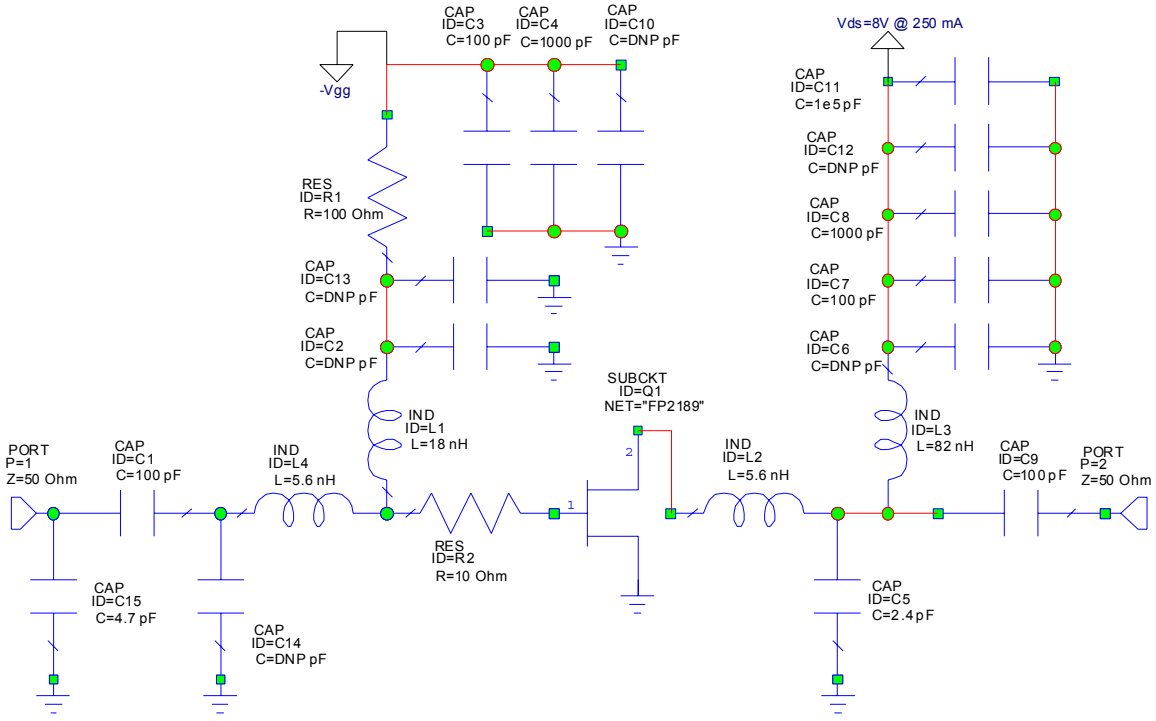
Specifications and information are subject to change without notice.

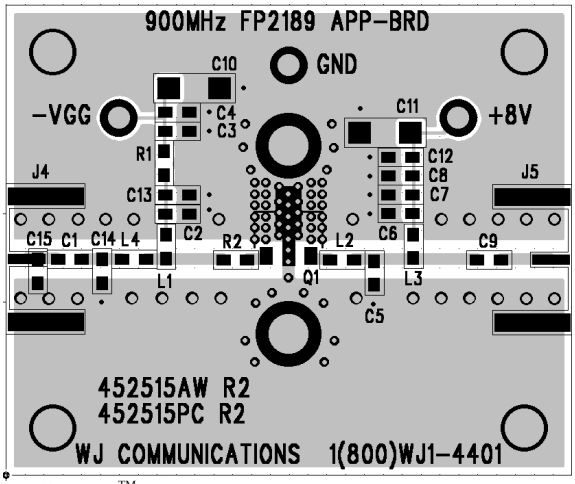
Application Circuit: 870 – 960 MHz (FP2189-PCB900S)

The application circuit is matched for output power.

Typical RF Performance
Drain Bias = +8 V, I_{ds} = 250 mA, 25°C

Frequency	MHz	870	915	960
S21 – Gain	dB	18.9	18.7	18.4
S11 – Input Return Loss	dB	-24	-21	-12
S22 – Output Return Loss	dB	-7.6	-8.3	-9.6
Output P1dB	dBm	+30.0	+30.2	+30.0
Output IP3 (+15 dBm / tone, 1 MHz spacing)	dBm		+42.8	
Noise Figure	dB	4.2	4.5	4.5
IS-95 Channel Power @ -45 dBc ACPR	dBm		+24.5	



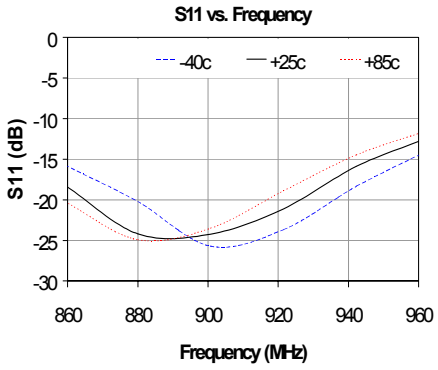


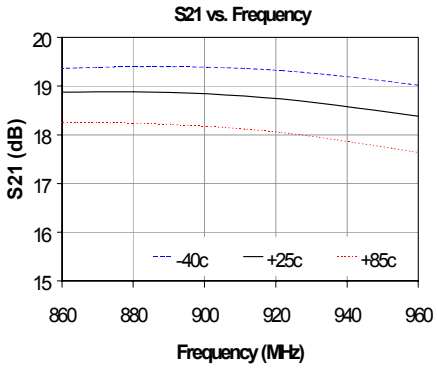
14 mil GETEK™ ML200DSS (εr = 4.2)
The main microstrip line has a line impedance of 50 Ω.

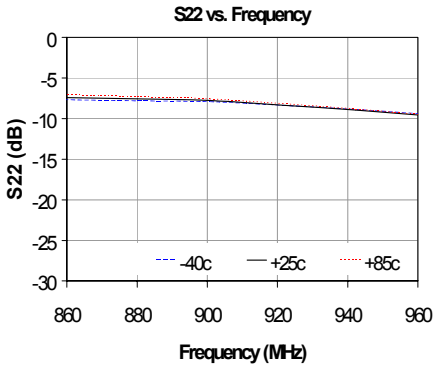
Bill of Materials

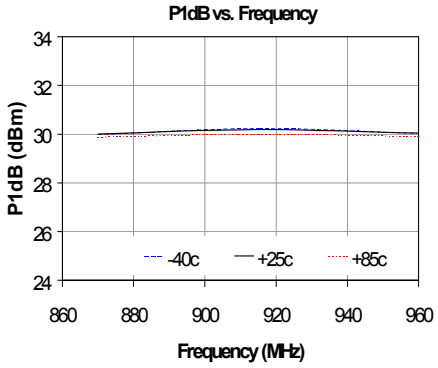
Ref. Desig.	Value	Part style	Size
C1, C3, C7, C9, C13	100 pF	Chip capacitor	0603
C4, C8	1000 pF	Chip capacitor	0603
C5	2.4 pF	Chip capacitor	0603
C11	0.1 µF	Chip capacitor	1206
L1	18 nH	Multilayer chip inductor	0603
L2, L4	5.6 nH	Multilayer chip inductor	0603
L3	82 nH	Multilayer chip inductor	0603
R1	100 Ω	Chip resistor	0603
R2	10 Ω	Chip resistor	0603
Q1	FP2189	WJ 1W HFET	SOT-89
C2, C6, C10, C12, C14		Do Not Place	

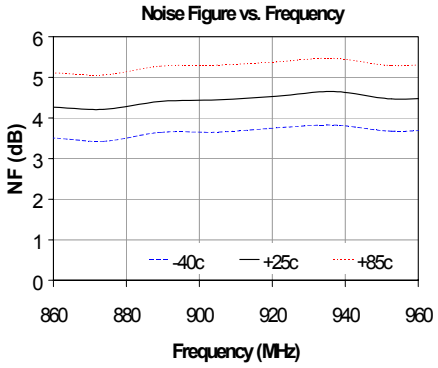
FP2189-PCB900S Application Circuit Performance Plots

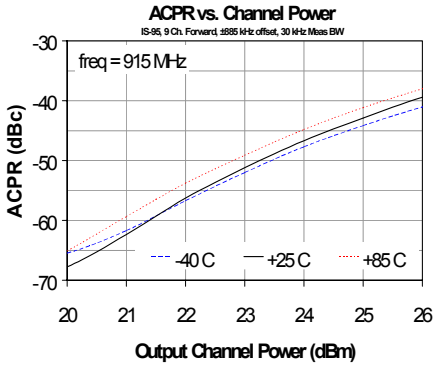


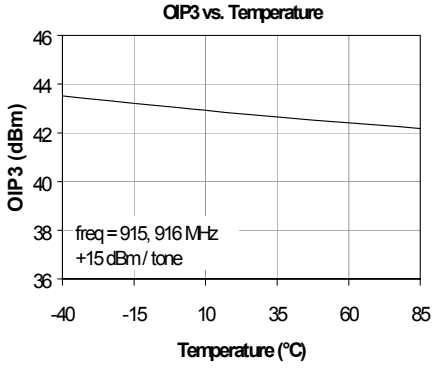


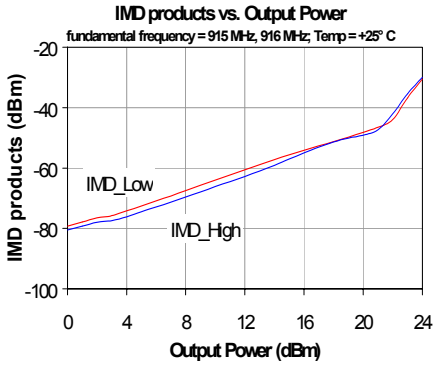


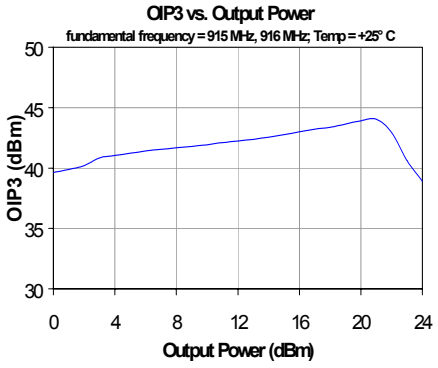


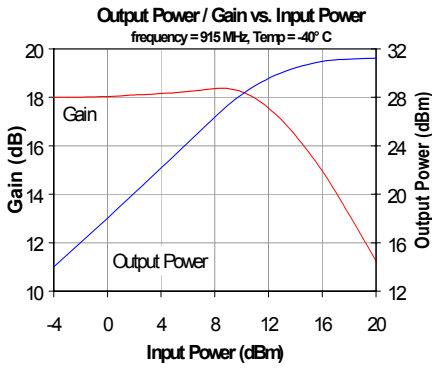


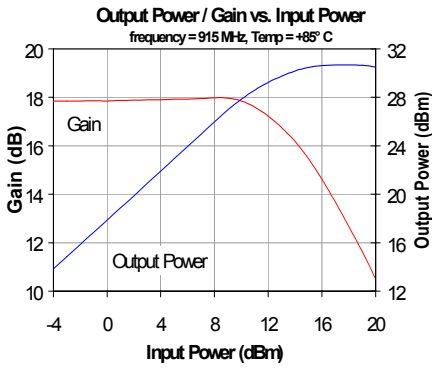


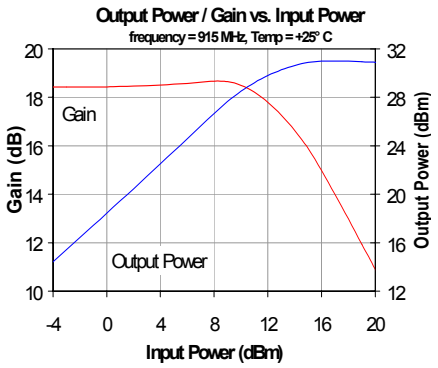










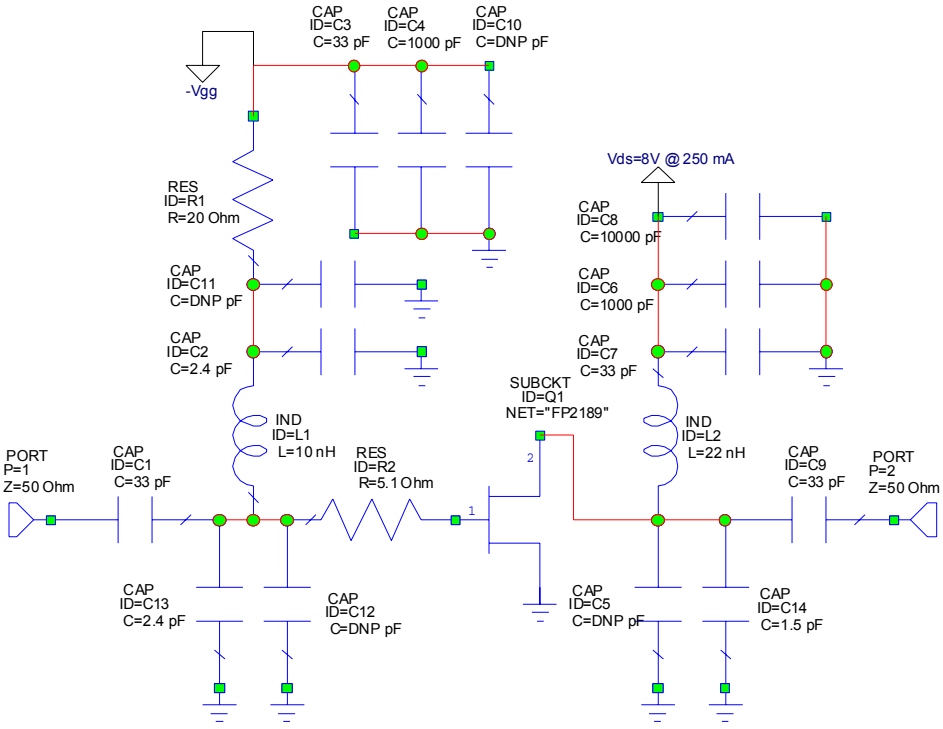


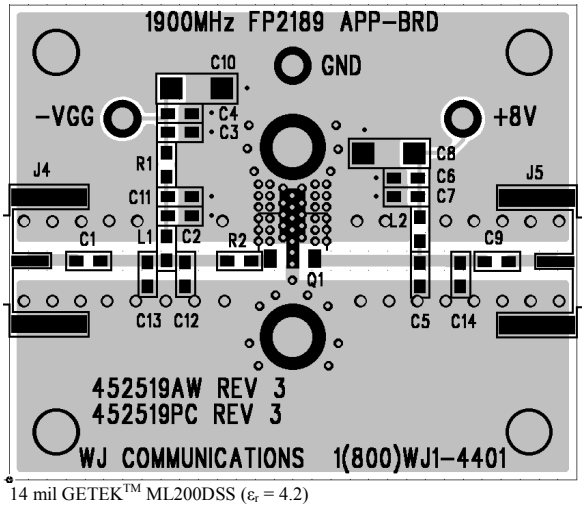
Application Circuit: 1930 – 1990 MHz (FP2189-PCB1900S)

The application circuit is matched for output power.

Typical RF Performance
Drain Bias = +8 V, I_{ds} = 250 mA, 25°C

Frequency	MHz	1930	1960	1990
S21 – Gain	dB	15.6	15.6	15.4
S11 – Input Return Loss	dB	-15.4	-14.6	-13.2
S22 – Output Return Loss	dB	-12	-12	-12
Output P1dB	dBm	+30.2	+30.4	+30.5
Output IP3 (+15 dBm / tone, 1 MHz spacing)	dBm		+43.5	
Noise Figure	dB	3.4	3.4	3.6
IS-95 Channel Power @ -45 dBc ACPR	dBm		+23.8	



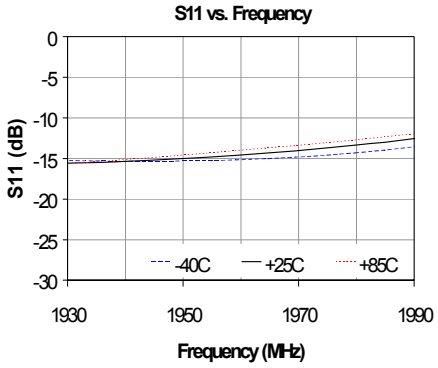


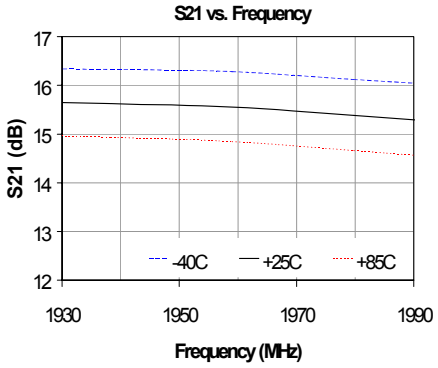
14 mil GETEK™ ML200DSS (ε_r = 4.2)
The main microstrip line has a line impedance of 50 Ω.

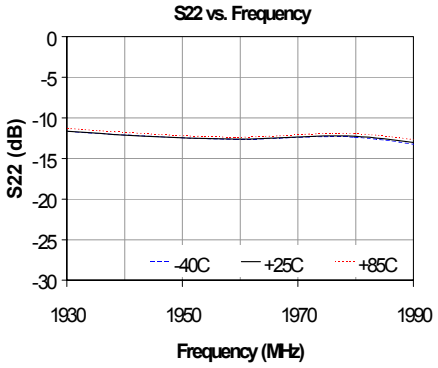
Bill of Materials

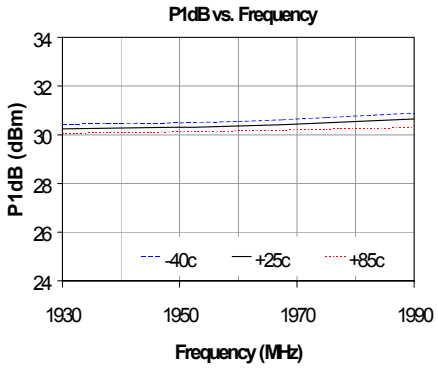
Ref. Desig.	Value	Part style	Size
C1, C3, C7, C9	100 pF	Chip capacitor	0603
C2, C13	2.4 pF	Chip capacitor	0603
C4, C6	1000 pF	Chip capacitor	0603
C8	0.1 µF	Chip capacitor	1206
C14	1.5 pF	Chip capacitor	0603
L1	10 nH	Multilayer chip inductor	0603
L2	22 nH	Multilayer chip inductor	0603
R1	20 Ω	Chip resistor	0603
R2	5.1 Ω	Chip resistor	0603
Q1	FP2189	WJ 1W HFET	SOT-89
C5, C10, C11, C12		Do Not Place	

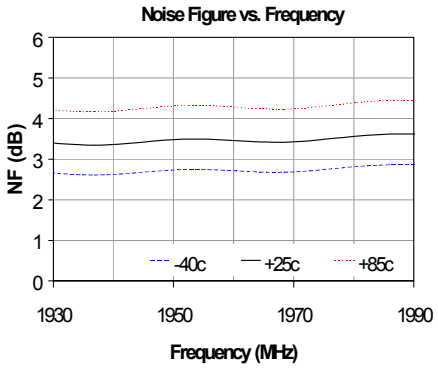
FP2189-PCB1900S Application Circuit Performance Plots

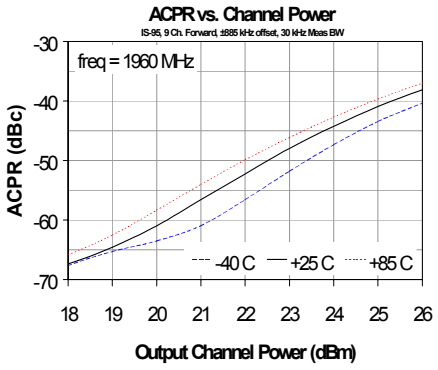


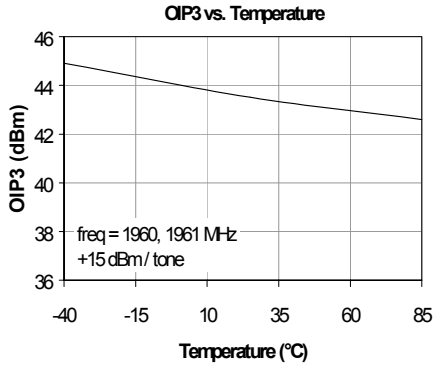


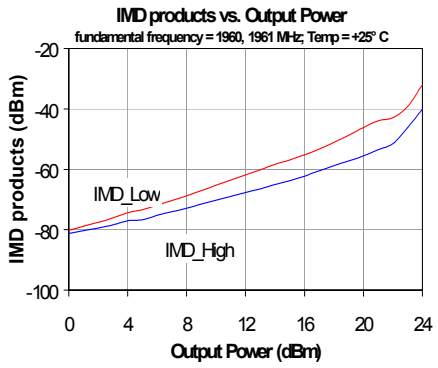


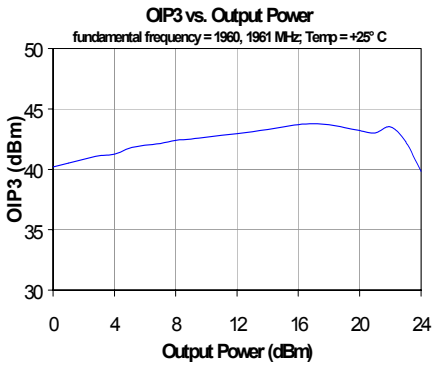


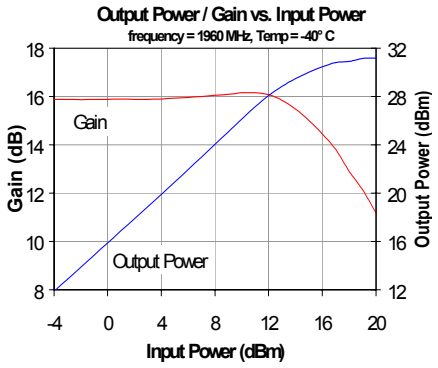


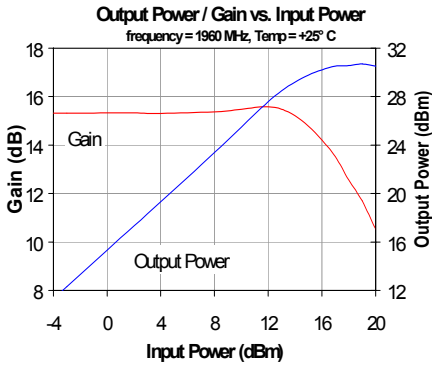


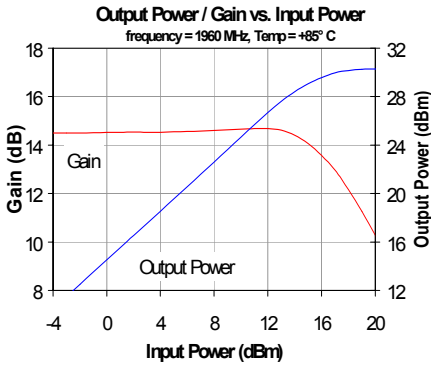










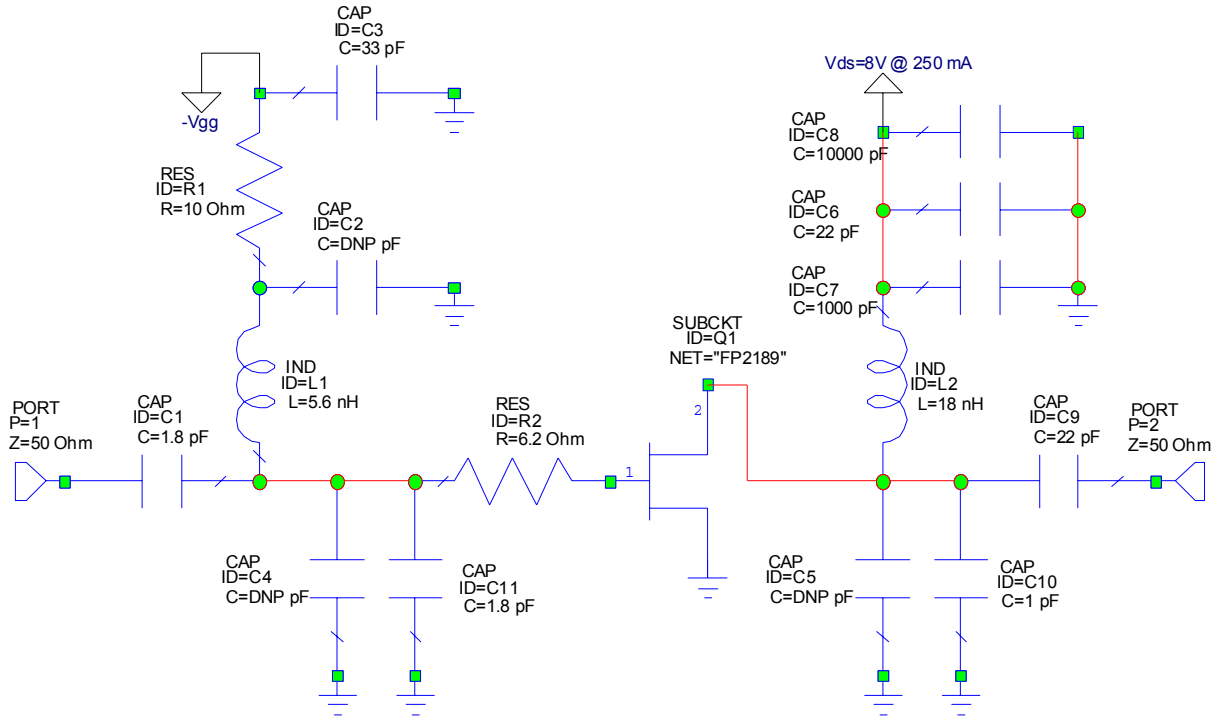


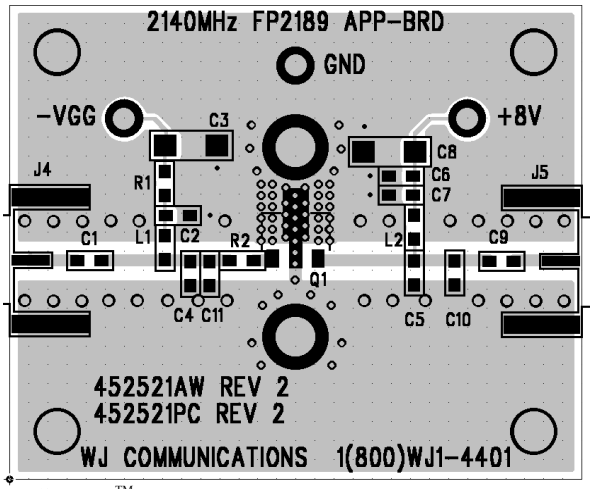
Application Circuit: 2110 – 2170 MHz (FP2189-PCB2140S)

The application circuit is matched for output power.

Typical RF Performance
Drain Bias = +8 V, I_{ds} = 250 mA, 25°C

Frequency	MHz	2110	2140	2170
S21 – Gain	dB	14.4	14.4	14.4
S11 – Input Return Loss	dB	-23	-23	-22
S22 – Output Return Loss	dB	-9.7	-11.5	-12
Output P1dB	dBm	+30.5	+30.6	+30.2
Output IP3 (+15 dBm / tone, 1 MHz spacing)	dBm		+43.9	
Noise Figure	dB	4.2	4.5	4.3
W-CDMA Channel Power @ -45 dBc ACPR	dBm		+22.2	



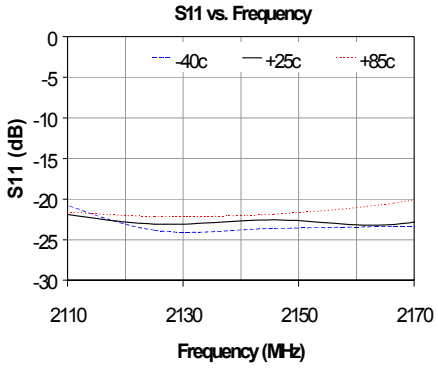


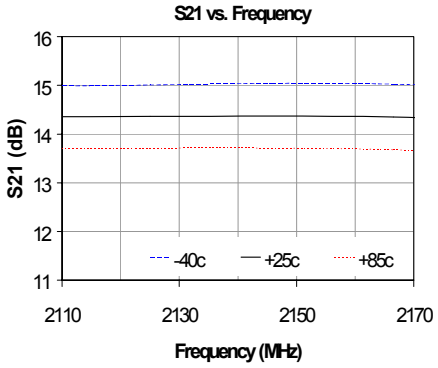
14 mil GETEK™ ML200DSS (ε_r = 4.2)
The main microstrip line has a line impedance of 50 Ω.

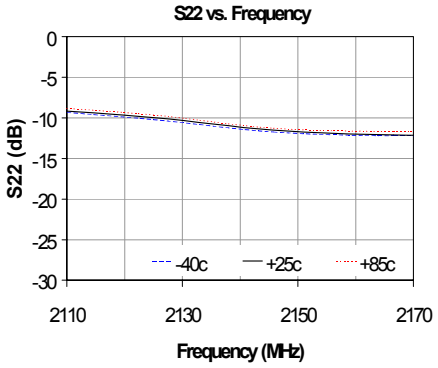
Bill of Materials

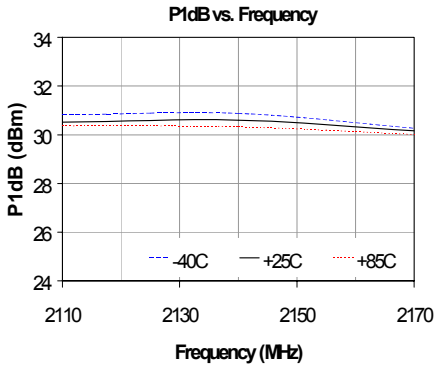
Ref. Desig.	Value	Part style	Size
C1, C11	1.8 pF	Chip capacitor	0603
C3	33 pF	Chip capacitor	0805
C6, C9	22 pF	Chip capacitor	0603
C7	1000 pF	Chip capacitor	0603
C8	0.1 µF	Chip capacitor	1206
C10	1.0 pF	Chip capacitor	0603
L1	5.6 nH	Multilayer chip inductor	0603
L2	18 nH	Multilayer chip inductor	0603
R1	10 Ω	Chip resistor	0603
R2	6.2 Ω	Chip resistor	0603
Q1	FP2189	WJ 1W HFET	SOT-89
C2, C4, C5		Do Not Place	

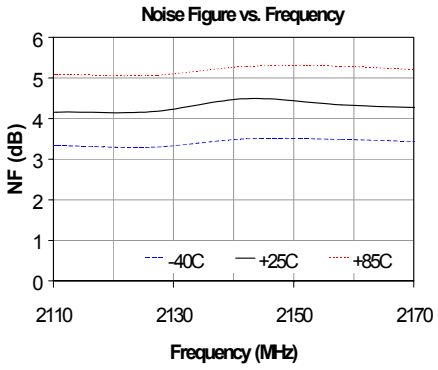
FP2189-PCB2140S Application Circuit Performance Plots

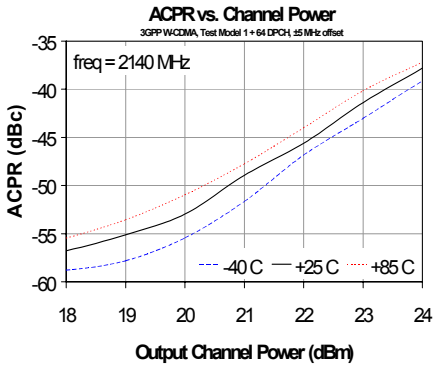


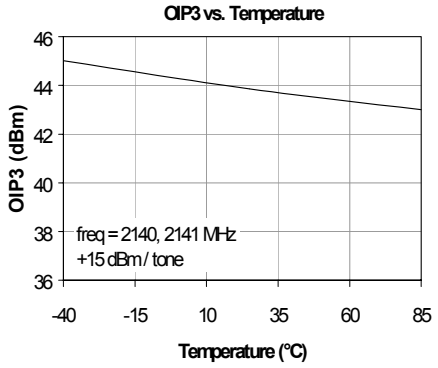


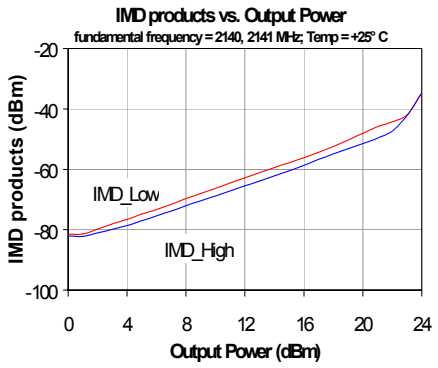


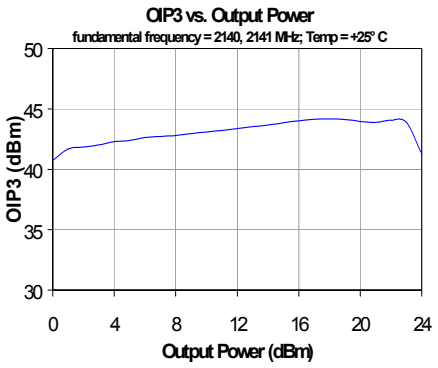


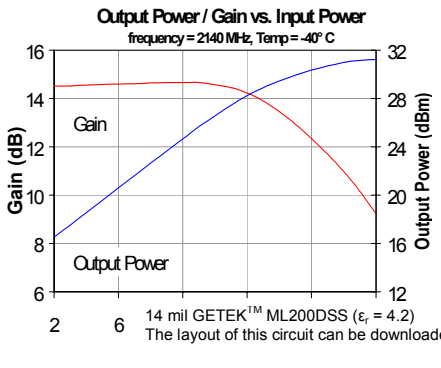


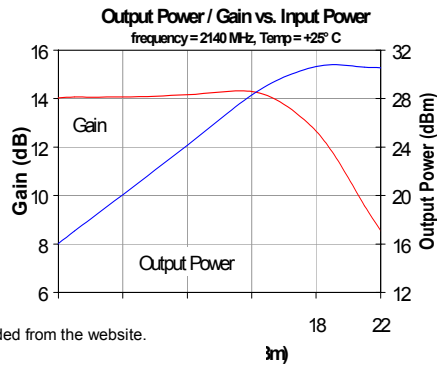


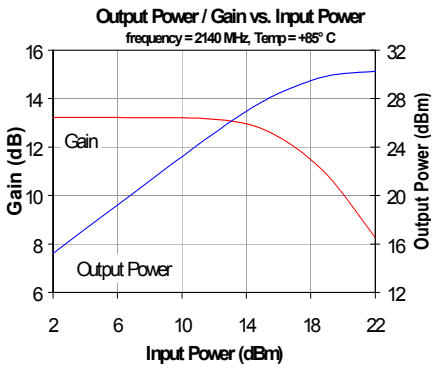












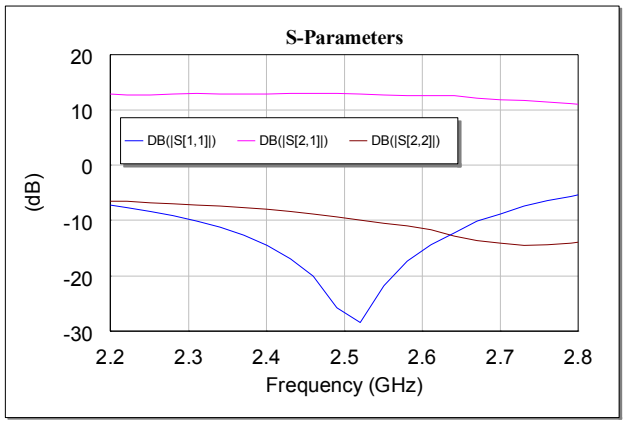
14 mil GETEK™ ML200DSS (ε_r = 4.2)
The layout of this circuit can be downloaded from the website.

Reference Design: 2400 – 2600 MHz

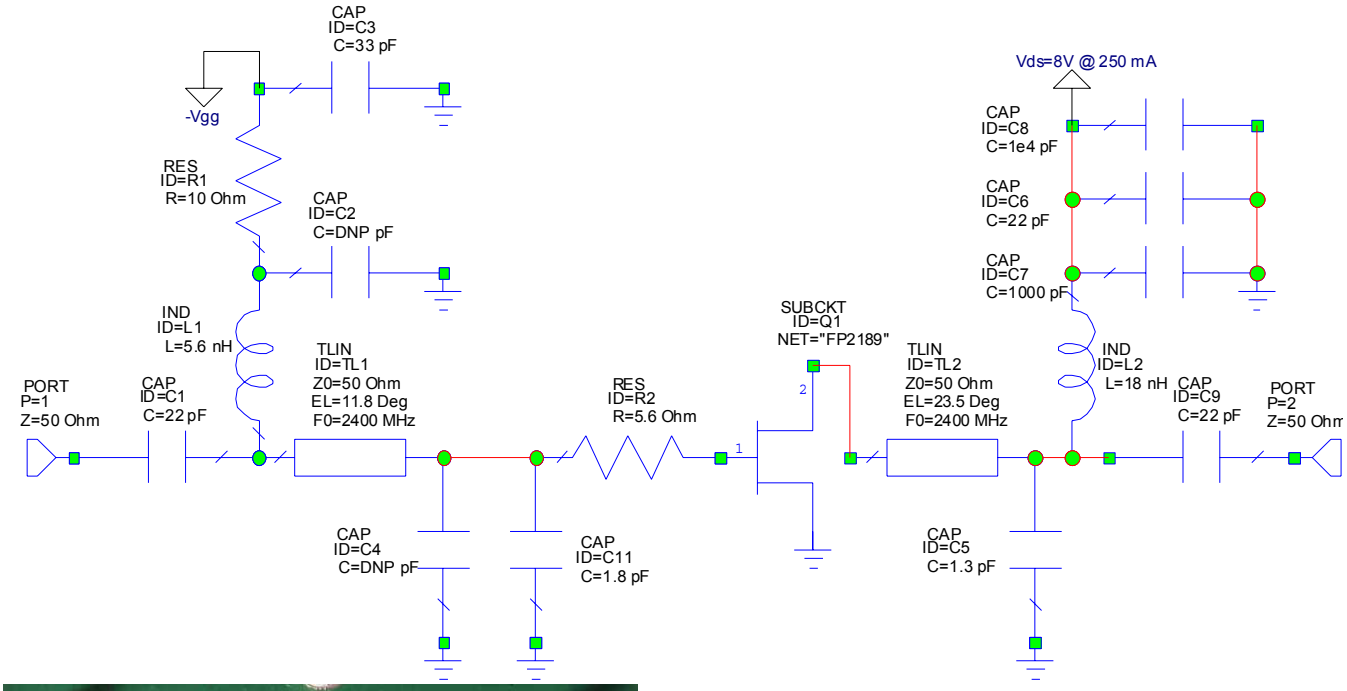
The application circuit is matched for output power.

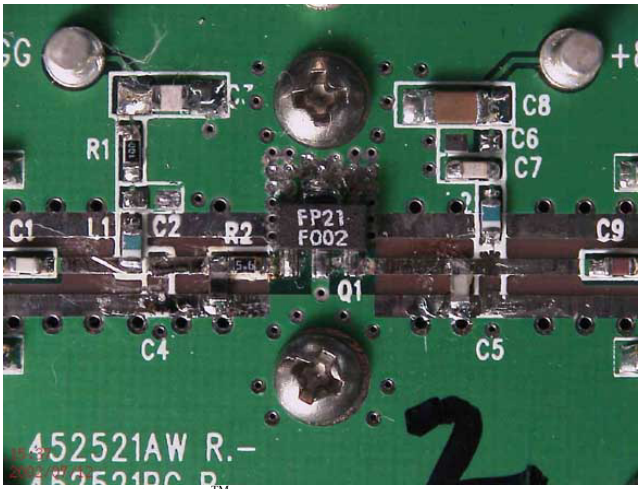
Typical RF Performance
Drain Bias = +8 V, I_{ds} = 250 mA, 25°C

Frequency	MHz	2400	2500	2600
S21 – Gain	dB	12.9	13.0	12.6
S11 – Input Return Loss	dB	-14.5	-26	-15
S22 – Output Return Loss	dB	-7.9	-9.6	-11.4
Output P1dB	dBm	+31.1	+31.2	+30.8
Output IP3 (+15 dBm / tone, 1 MHz spacing)	dBm	+45.0	+45.3	+47.0



The 2.4 – 2.6 GHz Reference Circuit is shown for design purposes only. An evaluation board is not readily available for this application. The reader can obtain an FP2189-PCB2140S evaluation board and modify it with the circuit shown to achieve the performance shown in this reference design.





14 mil GETEK™ ML200DSS (ε_r = 4.2)
The main microstrip line has a line impedance of 50 Ω.

Bill of Materials

Ref. Desig.	Value	Part style	Size
C1, C6, C9	22 pF	Chip capacitor	0603
C3	33 pF	Chip capacitor	0805
C5	1.3 pF	Chip capacitor	0603
C11	1.8 pF	Chip capacitor	0603
C7	1000 pF	Chip capacitor	0603
C8	0.1 µF	Chip capacitor	1206
L1	5.6 nH	Multilayer chip inductor	0603
L2	18 nH	Multilayer chip inductor	0603
R1	10 Ω	Chip resistor	0603
R2	5.6 Ω	Chip resistor	0603
Q1	FP2189	WJ 1W HFET	SOT-89
C2, C4		Do Not Place	

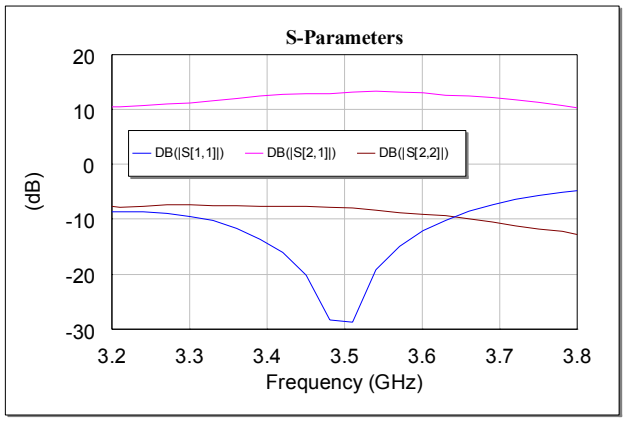
Reference Design: 3400 – 3600 MHz

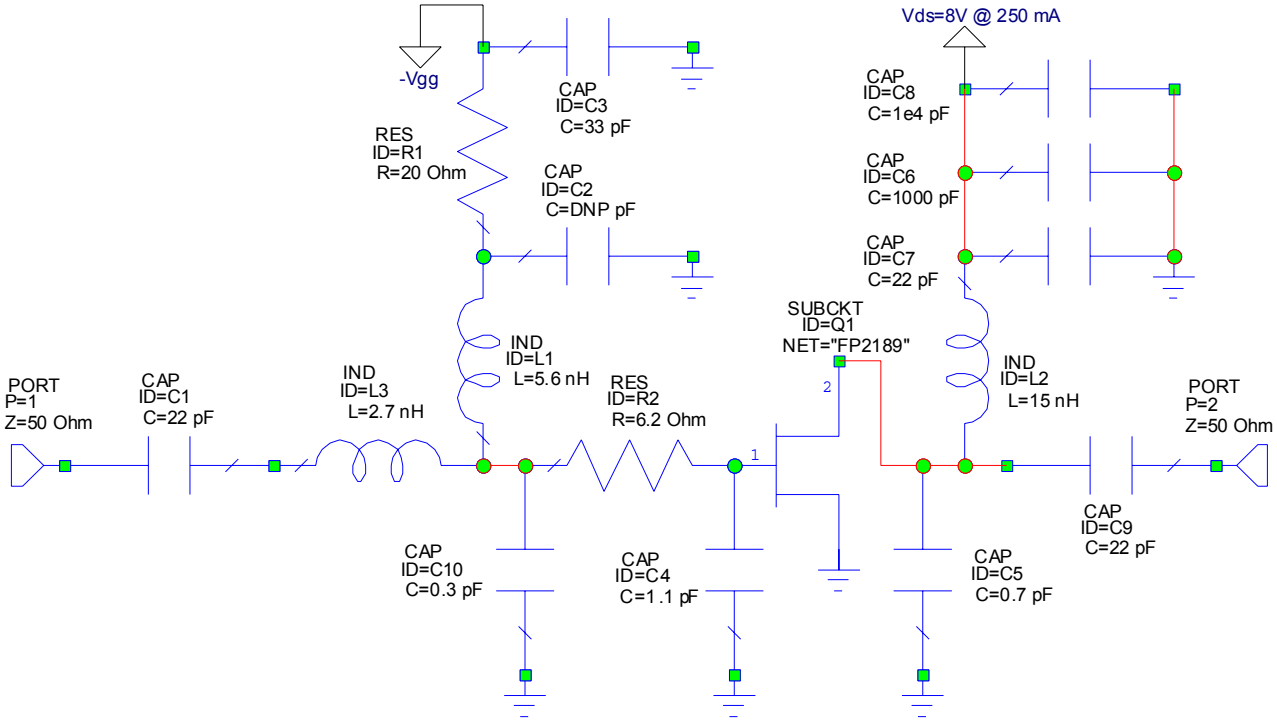
The application circuit is matched for output power.

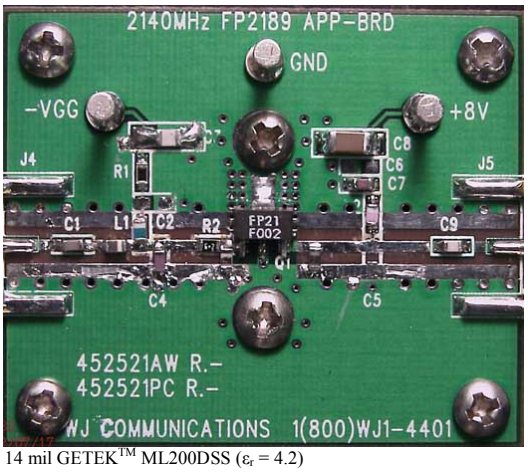
Typical RF Performance
Drain Bias = +8 V, I_{ds} = 250 mA, 25°C

Frequency	MHz	3400	3500	3600
S21 – Gain	dB	12.6	13.0	12.9
S11 – Input Return Loss	dB	-15	-28	-12
S22 – Output Return Loss	dB	-7.6	-7.9	-9.1
Output P1dB	dBm	+30.9	+30.9	+30.8
Output IP3 (+15 dBm / tone, 1 MHz spacing)	dBm	+43.8	+43.6	+43.8

The 3.4 – 3.6 GHz Reference Circuit is shown for design purposes only. An evaluation board is not readily available for this application. The reader can obtain an FP2189-PCB2140S evaluation board and modify it with the circuit shown to achieve the performance shown in this reference design.







14 mil GETEK™ ML200DSS (ε_r = 4.2)
The main microstrip line has a line impedance of 50 Ω.

Bill of Materials

Ref. Desig.	Value	Part style	Size
C1, C7, C9	22 pF	Chip capacitor	0603
C3	33 pF	Chip capacitor	0805
C4	1.1 pF	Chip capacitor	0603
C5	0.7 pF	Chip capacitor	0603
C6	1000 pF	Chip capacitor	0603
C8	0.1 µF	Chip capacitor	1206
C10	0.3 pF	Chip capacitor	0603
L1	5.6 nH	Multilayer chip inductor	0603
L2	15 nH	Multilayer chip inductor	0603
L3	2.7 nH	Multilayer chip inductor	0603
R1	20 Ω	Chip resistor	0603
R2	6.2 Ω	Chip resistor	0603
Q1	FP2189	WJ 1W HFET	SOT-89
C2		Do Not Place	

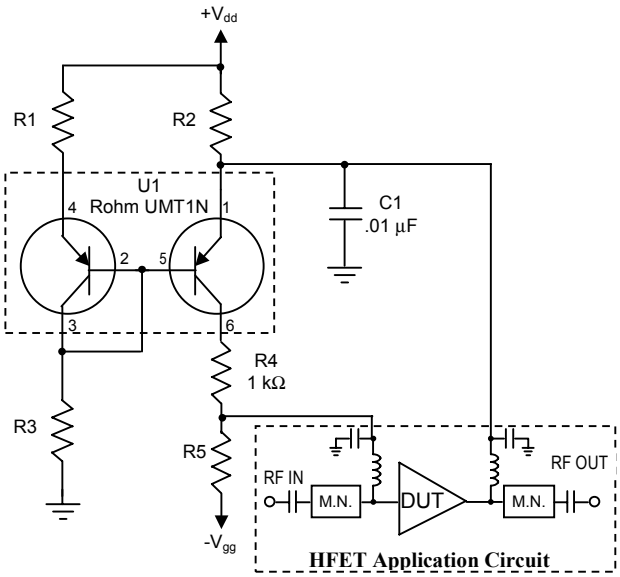
Application Note: Constant-Current Active-Biasing

Special attention should be taken to properly bias the FP2189. Power supply sequencing is required to prevent the device from operating at 100% Idss for a prolonged period of time and possibly causing damage to the device. It is recommended that for the safest operation, the negative supply be "first on and last off." With a negative gate voltage present, the drain voltage can then be applied to the device. The gate voltage can then be adjusted to have the device be used at the proper quiescent bias condition.

An optional active-bias current mirror is recommended for use with the application circuits shown in this datasheet. Generally in a laboratory environment, the gate voltage is adjusted until the drain draws the recommended operating current. The gate voltage required can vary slightly from device to device because of device pinchoff variation, while also varying slightly over temperature.

The active-bias circuit, shown on the right, uses dual PNP transistors to provide a constant drain current into the FP2189, while also eliminating the effects of pinchoff variation. This configuration is best suited for applications where the intended output power level of the amplifier is backed off at least 6 dB away from its compression point. With the implementation of the circuit, lower P1dB values may be measured for a Class-AB amplifier, where the device will attempt to source more drain current while the circuit tries to provide a constant drain current. The circuit should be connected directly in line with where the voltage supplies would be normally connected with the amplifier circuit, as shown the diagram. Any required matching circuitry remains the same, although it is not shown in the diagram. This recommended active-bias constant-current circuit adds 7 components to the parts count for implementation, but should cost only an extra $0.144 to realize ($0.10 for U1, $0.0029 for R1, R3, R4, R5, $0.024 for R2, and $0.0085 for C1).

Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the two PNP transistors. As a 1st order approximation, this is achieved by using matched transistors with approximately the same Ibe current. Thus the transistor emitter voltage adjusts the HFET gate voltage so that the device draws a constant current, regardless of the temperature. A Rohm dual transistor - UMT1N - is recommended for cost, minimal board space requirements, and to minimize the variation between the two transistors. Minimizing the variability between the base-to-emitter junctions allow more accuracy in setting the current draw. More details can be found in a separate application note "Active-bias Constant-current Source Recommended for HFETs" found on the WJ website.



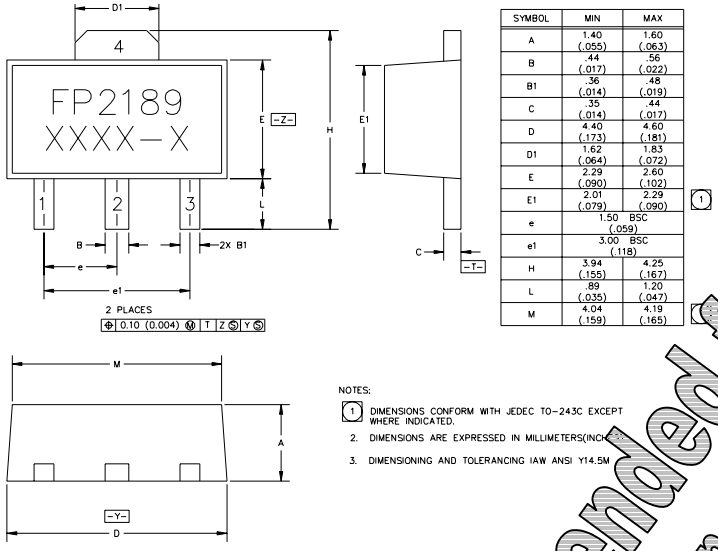
Parameter	FP2189
Pos Supply, Vdd	+8 V
Neg Supply, Vgg	-5 V
Vds	+7.75 V
Ids	250 mA
R1	62 Ω
R2	1.0 Ω
R3	1.8 kΩ
R4	1 kΩ
R5	1 kΩ

*R2 should be of size 0805 to dissipate 0.0625 Watts. This should be of 1% tolerance. Two 2.0 Ω resistors in parallel of size 0603 can also be used.

FP2189 (SOT-89 Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing



SYMBOL	MIN	MAX
A	1.40 (.055)	1.60 (.063)
B	.44 (.017)	.56 (.022)
B1	.36 (.014)	.48 (.019)
C	.35 (.014)	.44 (.017)
D	4.40 (.173)	4.60 (.181)
D1	1.62 (.064)	1.83 (.072)
E	2.29 (.090)	2.60 (.102)
E1	2.01 (.079)	2.29 (.090)
e	1.50 BSC (.059)	
e1	3.00 BSC (.118)	
H	3.94 (.155)	4.25 (.167)
L	.89 (.035)	1.20 (.047)
M	4.04 (.159)	4.19 (.165)

Product Marking

The FP2189 will be marked with an "FP2189" designator. An alphanumeric lot code ("XXXX-X") is also marked below the part designator on the top surface of the package.

Tape and reel specifications for this part are located on the web site in the "Application Notes" section.

MSL / ESD Rating

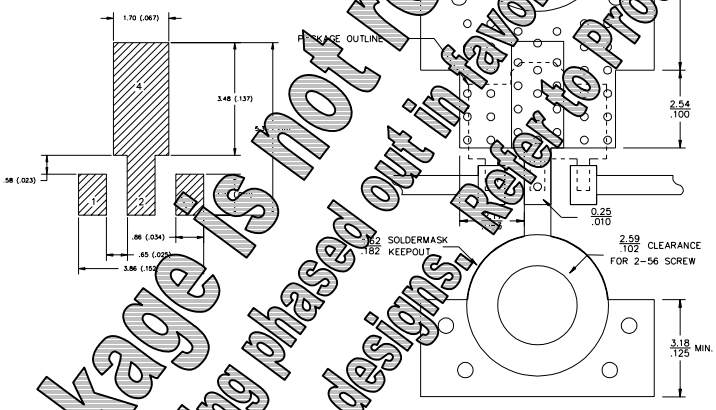
Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes /500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes at 2000 V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +235° C convection reflow
Standard: JEDEC Standard J-STD-020

Land Pattern



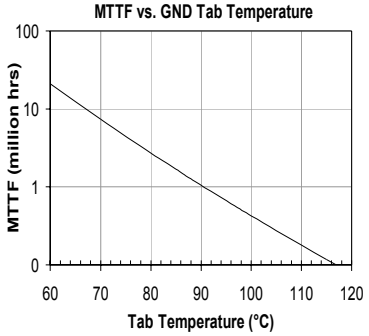
Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85°C
Thermal Resistance, Rth (1)	35° C/W
Junction Temperature, Tj (2)	155° C

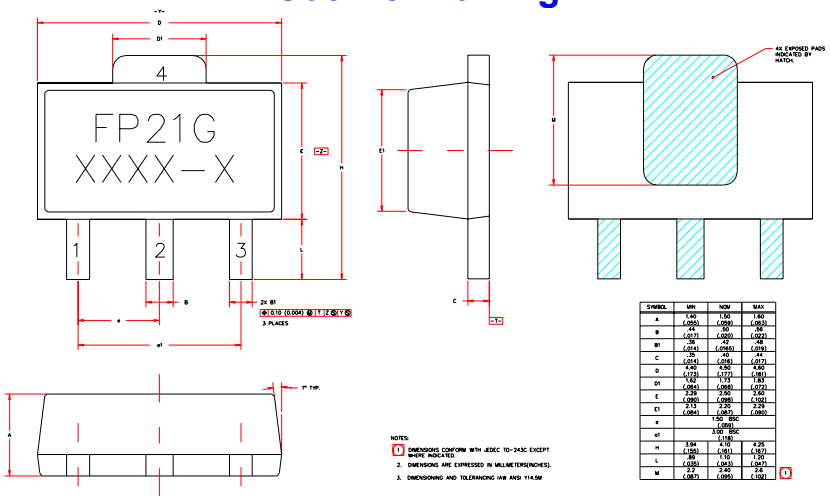
1. The thermal resistance is referenced from the hottest part of the junction to the ground tab (pin 4).
2. This corresponds to the typical drain biasing condition of 5V, 250 mA and an 85°C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160 °C.



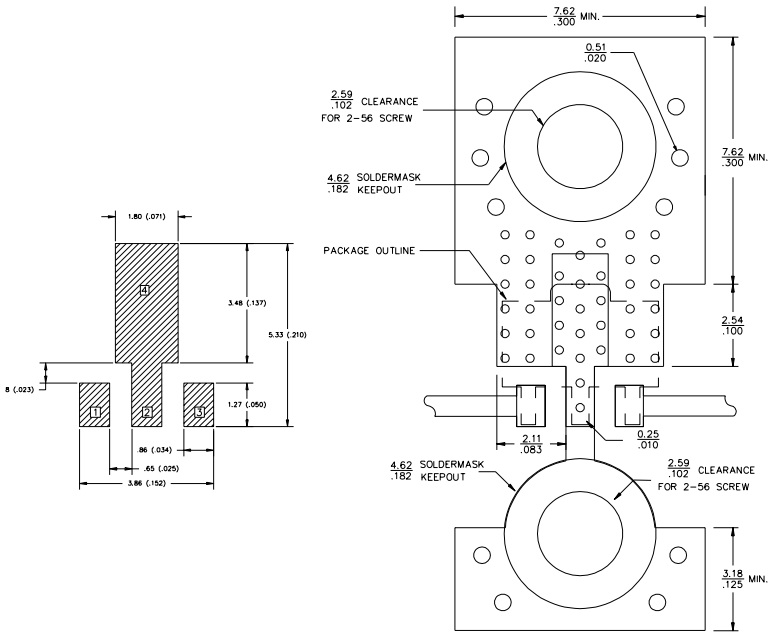
FP2189-G (Green / Lead-free SOT-89 Package) Mechanical Information

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

Outline Drawing



Land Pattern



Product Marking

The FP2189-G will be marked with an "FP21G" designator. An alphanumeric lot code ("XXXX-X") is also marked below the part designator on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes /500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Rating:	Class IV
Value:	Passes at 2000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 3 at +260° C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85°C
Thermal Resistance, Rth (1)	35° C/W
Junction Temperature, Tjc (2)	155° C

1. The thermal resistance is referenced from the hottest part of the junction to the ground tab (pin 4).
2. This corresponds to the typical drain biasing condition of +8V, 250 mA at an 85°C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160 °C.